

**AMENDMENTS TO THE DRAWINGS:**

Please enter the attached New Figs. 26-32.

The circuit diagram shows a differential amplifier with a cross-coupled core. The core consists of two PMOS transistors (10, 20) and two NMOS transistors (1, 2). The gates of PMOS 10 and 20 are connected to a common bias voltage AVD. The gates of NMOS 1 and 2 are connected to a common bias voltage AVS. The drains of PMOS 10 and 20 are connected to a common supply voltage CK. The sources of NMOS 1 and 2 are connected to a common source voltage C C S. The gates of NMOS 1 and 2 are also connected to the drains of PMOS 10 and 20, respectively, forming a cross-coupled structure. The outputs of the amplifier are labeled q<sub>x</sub> and q<sub>y</sub>. The inputs are labeled CK and CK. The bias voltages AVD and AVS are indicated by triangles pointing to the gates of the PMOS and NMOS transistors, respectively. The source voltage C C S is indicated by a triangle pointing to the common source connection. The output voltages q<sub>x</sub> and q<sub>y</sub> are indicated by triangles pointing to the output nodes. The input voltages CK and CK are indicated by triangles pointing to the input nodes. The bias voltages AVD and AVS are indicated by triangles pointing to the gates of the PMOS and NMOS transistors, respectively. The source voltage C C S is indicated by a triangle pointing to the common source connection. The output voltages q<sub>x</sub> and q<sub>y</sub> are indicated by triangles pointing to the output nodes. The input voltages CK and CK are indicated by triangles pointing to the input nodes.

The circuit diagram shows a differential amplifier. At the top, a differential input stage consists of two PMOS transistors (10 and 20) and two NMOS transistors (11 and 21). The gates of PMOS 10 and 20 are connected to a common clock signal CK. The gates of NMOS 11 and 21 are connected to a common clock signal CK. The sources of PMOS 10 and 20 are connected to a common AVD supply. The sources of NMOS 11 and 21 are connected to a common AVS supply. The drains of PMOS 10 and 20 are connected to the gates of NMOS 11 and 21, respectively. The drains of NMOS 11 and 21 are connected to the gates of PMOS 20 and 10, respectively. The outputs of this stage are labeled q<sub>x</sub> and q. Below this stage is a cross-coupled core consisting of two PMOS transistors (1 and 2) and two NMOS transistors (30 and 30'). The gates of PMOS 1 and 2 are connected to a common clock signal CK. The gates of NMOS 30 and 30' are connected to a common clock signal CK. The sources of PMOS 1 and 2 are connected to a common AVD supply. The sources of NMOS 30 and 30' are connected to a common AVS supply. The drains of PMOS 1 and 2 are connected to the gates of NMOS 30' and 30, respectively. The drains of NMOS 30 and 30' are connected to the gates of PMOS 2 and 1, respectively. The outputs of this stage are labeled d and dx. A central node between the two stages is connected to a common clock signal CK.



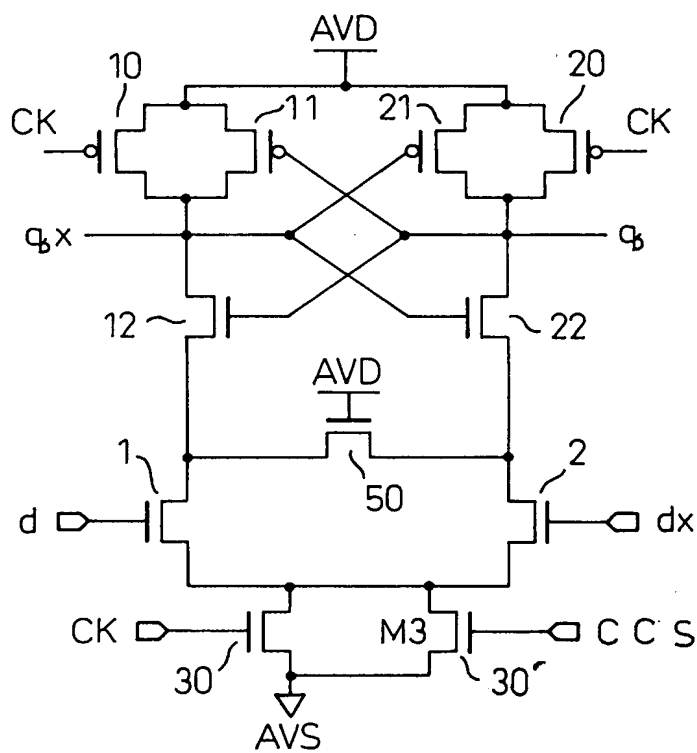
Application No. 10/072,872  
Amdt. Dated: June 1, 2004  
Reply to Office Action of December 1, 2003  
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Fig.28





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Fig. 29.

